CSCI 2330 – Caching Exercises

1. Consider a fully associative cache of effective size C, where S is the number of sets, E is the number of lines per set, and B is the block size. Write an expression for E in terms of S, B, and/or C.

2. Consider a hypothetical system containing only L1 cache and main memory. Assume that accessing L1 cache takes 1 cycle, while accessing memory takes an additional 100 cycles (i.e., 101 cycles total).

(a) You write a program and run it on this machine. Assuming the program exhibits a 97% cache hit rate, calculate the average number of cycles required to service each data access.

(b) Later, you restructure your program's loops to improve its locality and find that the cache hit rate slightly increases to 99%. Calculate the new average number of cycles required to service each data access. How does this compare to the previous access time? Was the slight increase in hit rate significant?

3. Consider a cache with (S, E, B) = (8, 2, 4), an 8-bit word size, and the partial contents shown below. In this cache, a single LRU bit indicates which line in each set was least recently used (LRU): if the LRU bit is 0, then the 1st line is LRU, while if the LRU bit is 1, then the 2nd line is LRU. For each of the following memory operations, (1) indicate whether a cache hit or miss occurs, and (2) draw the relevant updated cache set. Assume that the cache is reset to the contents shown below before each operation.

a. Read 11100100 (Value: 9)
b. Read 11100010 (Value: 17)
c. Write 01100100 (Value: 7)
d. Read 01000110 (Value: 5)
e. Write 01100000 (Value: 2)

Set #	LRU	V	D	Tag	Data (4 Bytes)	V	D	Tag	Data (4 Bytes)
0	1	0	0	111	4	1	0	001	17
1	0	1	1	111	9	1	0	010	5
2				…	…			…	…
3									
4									
5									
6									
7									