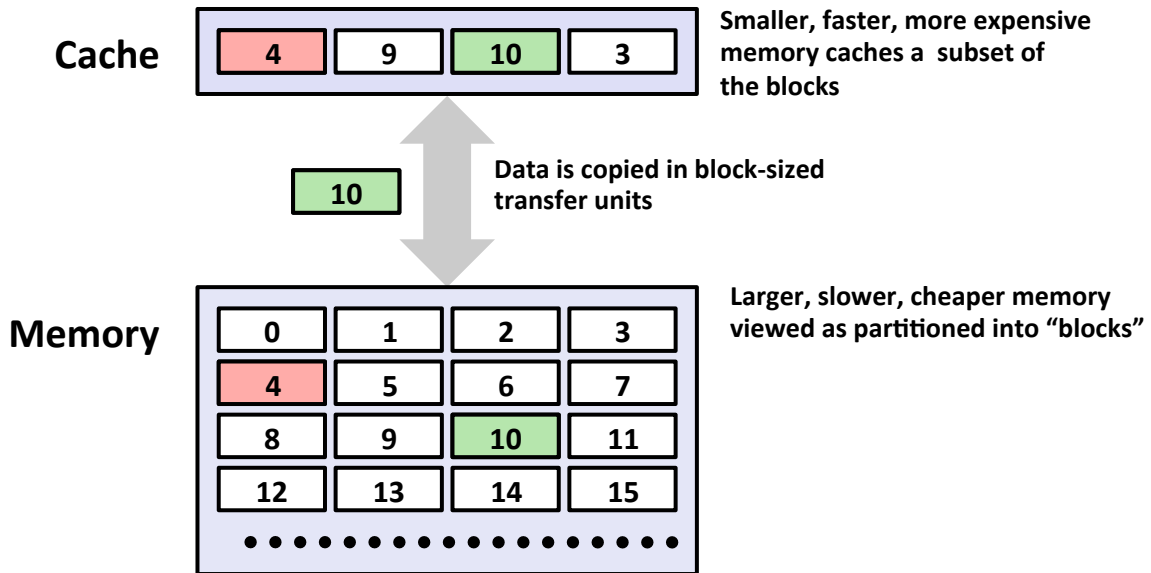
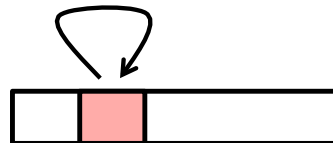


Caches

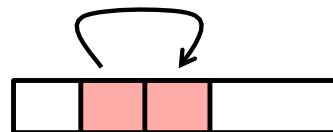


Locality

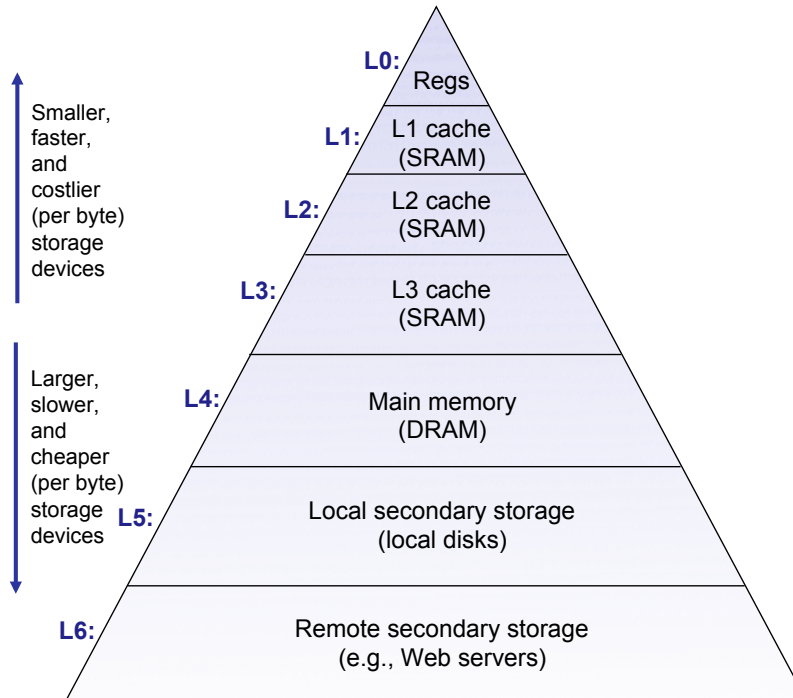
■ **Temporal locality:**



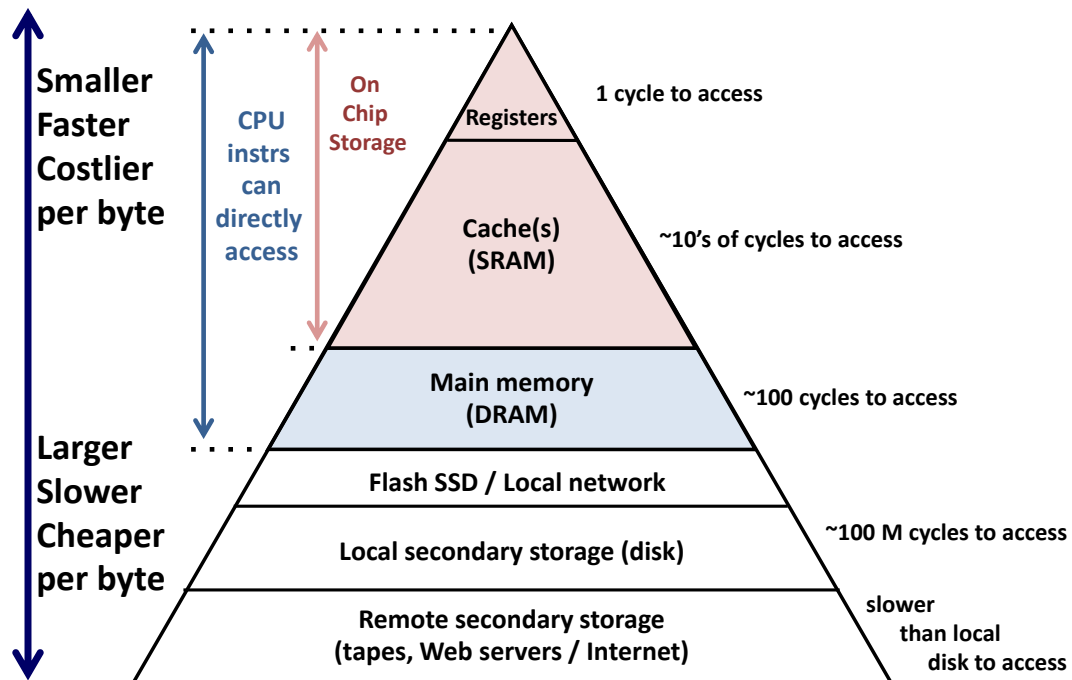
■ **Spatial locality:**



The Memory Hierarchy



The Memory Hierarchy (detail)



Direct-Mapped Cache

Line	V	D	Tag	Data (8 Bytes)
0				
1				
2				
3				
4				
...			...	
1020				
1021				
1022				
1023				

Direct-Mapped Address Components

(32-bit example)

Tag (19 bits)	Index (10 bits)	Byte offset (3 bits)



Line	V	D	Tag	Data (8 Bytes)
0				
1				
2				
3				
4				
...			...	
1020				
1021				
1022				
1023				

Direct-Mapped Exercise

Memory address



- Read 01000100 (Value: 5)
- Read 11100010 (Value: 17)
- Write 01110000 (Value: 7)
- Read 10101010 (Value: 12)
- Write 01101100 (Value: 2)

Line	V	D	Tag	Data (4 Bytes)
0	1	0	111	17
1	1	0	011	9
2	0	0	101	15
3	1	1	001	8
4	1	0	011	4
5	0	0	111	6
6	0	0	101	32
7	1	0	110	3

Direct-Mapped Exercise

Memory address



- Read 01000100 (Value: 5)
- Read 11100010 (Value: 17)
- Write 01110000 (Value: 7)
- Read 10101010 (Value: 12)
- Write 01101100 (Value: 2)

Line	V	D	Tag	Data (4 Bytes)
0	1	0	111	17
1	1	0	011 010	9 5
2	0 1	0	101 101	15 12
3	1	1 1	001 011	8 2
4	1	0 1	011	4 7
5	0	0	111	6
6	0	0	101	32
7	1	0	110	3