

CSCI 3310 – Address Translation Exercises

Consider a machine with a total memory size of 256 bytes, a page size of 16 bytes, and the (partial) page table shown below:

Page	Frame
0	2
1	6
2	11
3	9
4	5
5	0
6	4
...	...

1. How many possible pages can a process have?
2. How many bits are in a virtual address?
3. How many bits of the virtual address are for **p** (page number) and for **d** (page offset)?
4. Translate virtual address 24 to its physical memory address. Do this in two ways: using the computationally expensive non-binary method, and then using the efficient binary method.

On most machines, each address corresponds to a specific byte of memory -- such machines are called **byte-addressable**. Some special-purpose machines, on the other hand, use a different model where each address corresponds to a **word** of memory (the 'natural' data size of the processor) -- these machines are called **word-addressable**, and on such machines, a word is the smallest addressable quantity instead of a byte.

5. Suppose we have the same memory system described previously running on a word-addressable machine with a 32-bit word size. Repeat questions 1 through 4 given this memory architecture. Remember that addresses are now in terms of words, not bytes. What set of **bytes** in physical memory does virtual address 24 reference?
6. Using this word-addressable machine, translate virtual address 13 to its physical memory address (again using both methods), and give the set of physical memory bytes that this corresponds to.