# Algorithms for GIS csci3225 

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## Memory-efficient algorithms

## (Standard) algorithm analysis

- Running time $=$ number of instructions in the RAM model of computation


## RAM model = abstract model of a machine

- all arithmetic/logic/control instructions
- every instruction takes 1 step
- each memory access takes 1 step
- memory is infinite (data always fits in memory)



## Algorithms run on real machines



## The memory hierarchy

## An Example Memory Hierarchy



## Example



Figure 2.1 The levels in a typical memory hierarchy in a server computer shown on top (a) and in a personal mobile device (PMD) on the bottom (b). As we move farther away from the processor, the memory in the level below becomes slower and larger. Note that the time units change by a factor of 109 -from picoseconds to milliseconds-and that the size units change by a factor of $10^{12}$-from bytes to terabytes. The PMD has a slower clock rate and smaller caches and main memory. A key difference is that servers and desktops use disk storage as the lowest level in the hierarchy while PMDs use Flash, which is built from EEPROM technology.

## The memory hierarchy



- At all levels, data is organized and moved in blocks/pages
- Each level acts as a "cache" for the next level (stores most recently used blocks)
- When CPU needs to do a memory access, it first checks if the block that contains that data is (already) in the cache
- cache hit: the block that contains the data item is in cache; read it from cache
- cache miss: the block that contains the data item is not in cache; read the block in cache (and, if necessary, evict a block to make space)
- cache replacement policy: OPT, LRU, FIFO, ..


## Why does it matter anyways? Aren't computers getting faster?



Figure 2.2 Starting with 1980 performance as a baseline, the gap in performance, measured as the difference in the time between processor memory requests (for a single processor or core) and the latency of a DRAM access, is plotted over time. Note that the vertical axis must be on a logarithmic scale to record the size of the processor-DRAM performance gap. The memory baseline is 64 KB DRAM in 1980, with a 1.07 per year performance improvement in latency (see Figure 2.13 on page 99). The processor line assumes a 1.25 improvement per year until 1986, a 1.52 improvement until 2000, a 1.20 improvement between 2000 and 2005, and no change in processor performance (on a per-core basis) between 2005 and 2010; see Figure 1.1 in Chapter 1.

## Refined algorithm analysis



- CPU analysis
- number of instructions
- Memory access analysis
- number of blocks transferred between levels of the memory hierarchy


## Memory access analysis: The ideal-cache model



- Consider only two levels of the memory hierarchy
- Cache size $\mathbf{M}$ bytes
- Cache block (line) size B bytes
- Assume LRU or FIFO block replacement
- Fully associative cache (a block can go anywhere
- Count only one direction (what goes in must come out)


Performance measure: number of cache misses

$$
Q(n)=Q(n, M, B)
$$

## Analysis in the ideal-cache model

```
Example: Scanning
```

```
//array a was initialized with n elements
```

//array a was initialized with n elements
sum =0
sum =0
for (i=0; i<n; j++)
for (i=0; i<n; j++)
sum += a[i]

```
    sum += a[i]
```


## Example: Scanning

```
//array a was initialized with n elements
sum =0
for (i=0; i<n; j++)
    sum += a[i]
```

Notation:

- n: array size
- M: cache size
- B: block size



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    sum += a[i]
```

Notation:

- n: array size
- M: cache size
- B: block size
$B=32$ bytes $=8$ ints

Total: O(n/B) cache misses

## Example: Random access

```
//array a was initialized with n elements
sum =0
for (i=0; i<n; i++)
    k = random() %n ;
    sum += a[k]
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```

Notation:

- n: array size
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- B: block size
cache:



## Memory-efficient algorithms

- Summary
- Sequential access: $O(n / B)$ cache misses
- Random accesses: O(n) cache misses
- Spatial locality
- If a memory location is accessed, it's likely that a nearby memory location will be accessed in the near future
- Temporal locality
- If a memory location is accessed, it's likely that the same location will be accessed again in the near future
- Memory-efficient algorithms need to improve (spatial and/or temporal) locality


## Matrix multiplication

Given two n-by-n matrices, compute their product


Three algorithms:

- standard
- blocked/tiling
- divide-and-conquer
- Illustrate the analysis and design of memory-efficient algorithms


## Matrix multiplication: standard

```
//we'll use linearized arrays for efficiency
c = (double*) calloc(sizeof(double), n*n)
void mmult(double* a, double* b, double*c, int n) {
    int i, j, k;
        for (i=0; i<n; i++)
        for (j=0; j<n; j++)
            for (k=0; k<n; k++)
                    //c[i][j] += a[i][k]*b[k][j]
            c[i*n+j] += a[i*n+k]*b[k*n+j]
    }
```


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//we'll use linearized arrays for efficiency
c = (double*) calloc(sizeof(double), n*n)
void mmult(double* a, double* b, double*c, int n) {
    int i, j, k;
        for (i=0; i<n; i++)
            for (j=0; j<n; j++)
            for (k=0; k<n; k++)
                    //c[i][j] += a[i][k]*b[k][j]
                        c[i*n+j] += a[i*n+k]*b[k*n+j]
    }
```

        CPU: \(0\left(n^{3}\right)\)
        cache-misses:
    
## Cache-miss analysis

```
c = (double*) calloc(sizeof(double), n*n)
void mmult(double* a, double* b, double*c, int n) {
    int i, j, k;
    for (i=0; i<n; i++)
        for (j=0; j<n; j++)
            for (k=0; k<n; k++)
                        c[i*n+j] += a[i*n+k]*b[k*n+j]
    }
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        for (j=0; j<n; j++)
            for (k=0; k<n; k++)
                    c[i*n+j] += a[i*n+k]*b[k*n+j]
    }
```


each element in c accesses a row of a ( $n / B$ blocks) and a column of $B$ ( $n$ blocks)

## Cache-miss analysis

```
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void mmult(double* a, double* b, double*c, int n) {
    int i, j, k;
    for (i=0; i<n; i++)
        for (j=0; j<n; j++)
            for (k=0; k<n; k++)
                        c[i*n+j] += a[i*n+k]*b[k*n+j]
    }
```


cache-misses: $0\left((n+n / B) n^{2}\right)=O\left(n^{3}\right)$
if $n<M / B$ : $b$ columns share same blocks $==>O\left(n^{3} / B\right)$

## Matrix multiplication:blocked

## Do it block by block, instead of element by element.



## Matrix multiplication:blocked



Partition the matrices in blocks of size r-by-r
Denote $\mathrm{C}_{\mathrm{ij}}$ : the r-by-r block with upper-left corner (i,j) Then $\mathrm{C}_{\mathrm{ij}}=\mathrm{A}_{\mathrm{i} 9} \mathrm{~B}_{0 \mathrm{j}}+\ldots$

## Matrix multiplication:blocked

```
c = (double*) calloc(sizeof(double), n*n)
void mmult(double* a, double* b, double*c, int n) {
    int i, j, k;
    for (i=0; i<n; i+=r)
        for (j=0; j<n; j+=r)
            //compute block of c with upper left corner at(i,j)
            for (k=0; k<n; k+=r)
```

                                \(/ / C_{i j}+=A_{i k} * B_{k j} \quad / /<\longrightarrow\) matrix multiplication
    
## Matrix multiplication:blocked

```
c = (double*) calloc(sizeof(double), n*n)
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    for (i=0; i<n; i+=r)
        for (j=0; j<n; j+=r)
    //compute block of c with upper left corner at(i,j)
    for (k=0; k<n; k+=r)
        //Computes Aik*B}\mp@subsup{\textrm{B}}{\textrm{kj}}{
        for (ij=i; ii<i+r; ij++)
            for (jj=j; jj<j+r; jj++)
        for (kk=k; kk<k+r; kk++)
                                c[ij*n+jj] += a[ij*n+kk]*b[kk*n+jj]
    }
```


## Cache-miss analysis



Notation:

- n: array size
- M: cache size
- B: block size

For each block of c: read $n / r$ blocks in a and $n / r$ blocks in $b$

In total there are (n/r)2 blocks in c

How to chose r?

## Cache-miss analysis



Notation:

- n: array size
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For each block of c:

```
read n/r blocks in a and n/r blocks in b
```

In total there are $(n / r)^{2}$ blocks in c

We'll chose the size of a block such that three blocks fit in cache: $3 r^{2}=\mathrm{M}$, or $r=$ Theta(sqrt M) •

How many cache misses to read a block of size r-by-r, in a matrix laid out in row-major order?


How many cache misses to read a block of size r-by-r, in a matrix laid out in row-major order?


How many blocks span a sub-matrix of size $r$-by-r, in a matrix laid out in row-major order?

How many cache misses to read a block of size r-by-r, in a matrix laid out in row-major order?


## A cache is called tall if $\mathrm{M}>\mathrm{B}^{2}$.



Reading a block of size M in a matrix laid out in row-major order takes $0(M / B)$ cache misses with the tall cache assumption.

If the cache is not tall, it takes $0(s q r t ~ M) ~ c a c h e ~ m i s s e s . ~$

## Cache-miss analysis



## Notation:

- n: array size
- M: cache size
- B: block size

Assume the size of a matrix block is chosen such that three blocks fit in cache: $3 r^{2}<M$, or $r=s q r t M$

For each block of c:
read $n / r$ blocks in a and $n / r$ blocks in $b$
In total there are $(n / r)^{2}$ blocks in c

A block has size $0(M)$ and reading it takes $0(M / B)$ misses with the tall cache assumption.

TOTAL: $(n / r)^{2} 2 n / r r^{2} / B$

## Cache-miss analysis



Notation:

- n: array size
- M: cache size
- B: block size

TOTAL: $0\left(n^{3} /(B\right.$ sqrt M))

The point is, it's much better (although messy to analyze)

## Summary

Notation:

- n: array size
- M: cache size
- B: block size

```
standard: 0(n3)
blocked: 0(n3/(B sqrt M))
```

Example:
cache block $B=32$ bytes $=4$ doubles
cache size $M=768$ elements $==>b=16$ elements
standard: $O\left(n^{3}\right)$
blocked: $O\left(n^{3} / 64\right)<--------64$ times fewer cache misses

```
standard: 0(n3)
blocked: O(n3/(B sqrt M))
```

Can we do better?

Matrix multiplication: divide \& conquer

## Matrix multiplication: divide \& conquer

Assume $n$ is a power of 2 .


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## Matrix multiplication: divide \& conquer

```
c = (double*) calloc(sizeof(double), n*n)
void mmult(double* a, double* b, double*c, int n) {
        //base case
        if (n==1)
            c = a*b
            return
    else
        compute mmult(a11, b11, p1, n/2)
        compute mmult(a12, b21, p2, n/2)
        compute a11b12 ...
        compute a12b22
        compute a21b11
        compute a22b21
        compute a21b12
        compute a22b22
        add p1+p2 and put it in c11
        add p3+p4 and put it in c12
        ...
    }
```

8 recursive calls to multiply matrices of size n/2-by-n/2

## Matrix multiplication: divide \& conquer

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```


## CPU analysis

- $\quad T(n)=2$ if $n=1$
- $\quad T(n)=8 T(n / 2)+n^{2}$ otherwise
solves to $O\left(n^{3}\right)$


## Notation:

## Matrix multiplication: divide \& conquer

- n: array size
- M: cache size
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        compute a21b11...
        compute a22b21...
        compute a21b12...
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    }
```


## Cache miss analysis

- $C(n)=8 C(n / 2)+O\left(n^{2} / B\right)$
- $\mathrm{C}(\mathrm{n})=$ ?? basecase


## Notation:

## Matrix multiplication: divide \& conquer

- n: array size
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Cache miss analysis:

- $C(n)=8 C(n / 2)+O\left(n^{2} / B\right)$
- $C(n)=$ ?? for basecase

What is a good base-case to analyze cache misses?
The recursive algorithm proceeds until matrix size $=1$.
Let $n$ ' be the size at which $a, b, c$ all fit in cache, ie $3 n^{\prime 2}=M$
From that point on, the algorithm keeps dividing and recursing. No matter in what order the elements of the matrices are brought in cache, once all blocks have been loaded, they stay in cache, since they fit in cache.
Reading a matrix of size $O(M)$ takes $O(M / B)$ with the tall cache assumption .
==> Basecase: $\mathrm{C}($ sqrt M$)=\mathrm{O}(\mathrm{M} / \mathrm{B})$

This solves to $O\left(n^{3} /(B\right.$ sqrt $M)$ ).

## Matrix layout

- a11, a12, ... b11, b12, ...are not contiguous in a. Reading a matrix of size r-by-r takes O(r2/B + r) misses, which is $O\left(r^{2} / B\right)$ with the tall cache assumption. However the $O(r)$ term will add to the constant factors.
- Can this be avoided?



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- Can this be avoided?


Yes, with a different matrix layout!
More on this next time

Notation:
Matrix multiplication: summary

- n: array size
- M: cache size
- B: block size

Cache miss analysis:

```
standard:
blocked:
    O(n3)
    O(n3/(B sqrt M))
divide-and-conquer: 0(n3/(B sqrt M))
```


## Matrix multiplication: summary

int i, j, k;
int i, j, k;
for (i=0; i<n; i+=r)
for (i=0; i<n; i+=r)
for (j=0; j<n; j+=r)
for (j=0; j<n; j+=r)
//compute block of c with upper
//left corner at(i,j)
for ( $k=0 ; k<n ; k+=r)$
$/ / C_{i j}+=A_{i k} * B_{k j}$
divide-and-conquer

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void mmult(double* a, double* b, double*c, int n) {
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    if (n==1)
        c = a*b
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            compute a12b22...
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            compute a22b21...
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            compute a22b22...
            add p1+p2 and put it in c11
            add p3+p4 and put it in c12
    }
```


## Matrix multiplication: summary


$0\left(n^{3} /(B\right.$ sqrt M) $)$
divide-and-conquer

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void mmult(double* a, double* b, double*c, int n) {
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## Notation:

## Aware or oblivious?

- n: array size
- M: cache size
- B: block size

Cache-aware algorithms
Cache-oblivious algorithms

- We use M and B to analyze it, but the algorithm does not need
knowledge of M and B


## Notation:

## Aware or oblivious?

- n: array size
- M: cache size
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Cache-aware algorithms
Cache-oblivious algorithms

- We use $M$ and $B$ to analyze it, but the algorithm does not need knowledge of M and B
- They are efficient at all levels of the memory hierarchy, simultaneously
- Elegant!


## Project1

- Implement the three algorithms for matrix multiplication
- 1. standard
- 2. blocked
- 3. divide-and-conquer
- For each algorithm, plot running time function of problem size n
- For the blocked algorithm, pick a large n and plot running time function of matrix block size r; chose the $r$ that optimizes running time
- Compare the algorithms and discuss your findings

Will be in GitHub soon!

## Resources

- Cache-oblivious algorithms were introduced by

Matteo Frigo, Charles E. Leiserson, Harald Prokop, Sridhar Ramachandran, "Cache-Oblivious Algorithms", FOCS'99 (pdf)

- Here are some links that may be helpful
- Charles Leiserson, MIT, lecture on cache-efficient algorithms (part of course Performance engineering of software systems). https://www.youtube.com/watch?v=T9LkSKK075M
- Erik Demaine, MIT, lecture on cache-oblivious median finding and matrix multiplication. It's long (1.5hr) but has all details in the analysis. https://www.youtube.com/watch?v=CSqbjfCCLrU
- cache-oblivious matrix multiply, part of Udacity course High-performance computing, 3min video, great for getting the essential, but misses the subtleties of the analysis, like the necessity of the tall-cache assumption. - (https://www.youtube.com/watch? $\mathrm{v}=\mathrm{vxk} \mathrm{ZkcbwU40}$


## Matrix layout



## row-major order

$$
\begin{array}{cccccccc}
0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 \\
8 & 9 & 10 & 11 & 12 & 13 & 14 & 15 \\
16 & 17 & 18 & 19 & 20 & 21 & 22 & 23 \\
24 & 25 & 26 & 27 & 28 & 29 & 30 & 31 \\
32 & 33 & 34 & 35 & 36 & 37 & 38 & 39 \\
40 & 41 & 42 & 43 & 44 & 45 & 46 & 47 \\
48 & 49 & 59 & 515253 & 54 & 55 \\
56 & 57 & 58 & 59 & 60 & 61 & 62 & 63
\end{array}
$$

## Matrix layout



## row-major order

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0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 \\
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24 & 25 & 26 & 27 & 28 & 29 & 30 & 31 \\
32 & 33 & 34 & 35 & 36 & 37 & 38 & 39 \\
40 & 41 & 42 & 43 & 44 & 45 & 46 & 47 \\
48 & 49 & 59 & 51 & 52 & 53 & 54 & 55 \\
56 & 57 & 58 & 59 & 60 & 61 & 62 & 63
\end{array}
$$

Show where the elements of $a_{11}$ reside in this array

## Matrix multiplication with blocked layout

```
c = (double*) calloc(sizeof(double), n*n)
void mmult(double* a, double* b, double*c, int n) {
        //base case
        if (n==1)
            c = a*b
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    else
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8 recursive calls to multiply matrices of size n/2-by-n/2

